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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANTS	:	Manoj Khare et al.
SERIAL NO.	:	09/749,660
FILED	:	December 28, 2000
FOR	:	METHOD AND APPARATUS FOR REDUCING MEMORY LATENCY IN A CACHE COHERENT MULTI-NODE ARCHITECTURE
GROUP ART UNIT	:	2186
EXAMINER	:	Tuan V. Thai
ASSIGNEE	:	INTEL CORPORATION

HON. COMMISSIONER
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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail and deposited with the U.S. Postal Service and addressed to: M/S: Non-Fee Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on

Dated: April 6, 2004 Signature Pilar Rodriguez
Pilar Rodriguez

AMENDMENT

S I R:

The following amendments and remarks below are respectfully submitted in response to the Office Action dated October 6, 2003.